

In the Claims

Claim 1 (Currently Amended) A reproduction signal processor comprising:

an analog/digital converter operable to sample for sampling an analog signal, and to convert ~~converting~~ the same into a ~~the~~ digital signal;

an automatic equalizer operable to perform for performing an automatic equalization of the digital signal;

a phase locked loop operable to generate for generating a reference clock which coincides with a phase included in the digital signal and reference frequency components; and

a frequency divider operable to generate for generating a frequency-divided clock obtained by performing integral multiplication of the period of the reference clock, and to output ~~outputting~~ the frequency-divided clock as an operation clock to said the analog/digital converter and said the automatic equalizer, wherein

the automatic equalizer comprises is composed of:

a transversal filter operable to perform for performing waveform equalization of the digital signal;

an a straight-line interpolation unit operable to interpolate for interpolating the omission of the sampling number due to the sampling using the frequency-divided clock in the output of said the transversal filter; and

a control unit operable to estimate for estimating an equalization target value in accordance with the output of said the transversal filter, and to control controlling a parameter of said the transversal filter to minimize such that an equalization error which is an error between the equalization target value and the output of said the transversal filter becomes minimum.

2. (Currently Amended) The reproduction signal processor of Claim 1, wherein said the straight-line interpolation unit is a straight-line interpolation unit and comprises composed of:

a flip-flop element operable to perform for performing a delay processing of an output equalization signal of said the transversal filter for one period of the frequency-divided clock; and

an adder operable to add for adding a signal after the delay processing and the output equalization signal.

3. (Currently Amended) The reproduction signal processor of Claim 1, wherein, said instead of the straight-line interpolation unit, is a high-order interpolation unit operable to interpolate for interpolating the omission of the sampling number due to the sampling using the frequency-divided clock in the output of said the transversal filter is provided.

4. (Currently Amended) The reproduction signal processor of Claim 3, wherein said the high-order interpolation unit comprises is composed of:

a flip-flop element operable to perform for performing delay processing for one period of the frequency-divided clock;

plural multipliers operable to perform for performing weighting of a tap coefficient on a signal after the delay processing; and

an adder operable to add for adding an output signal of said the plural multipliers.